Figure 1

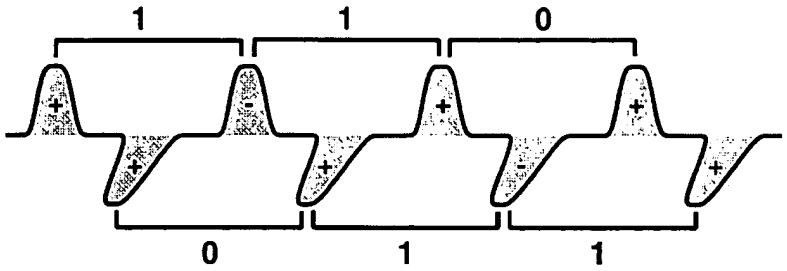


Figure 2

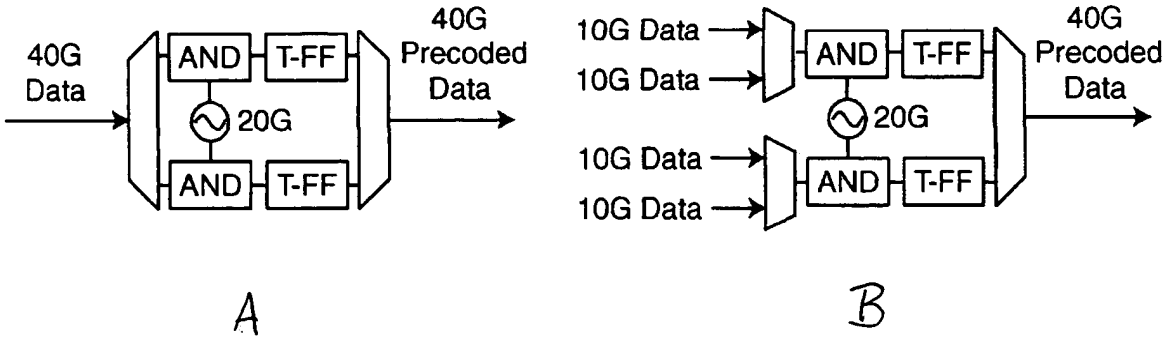
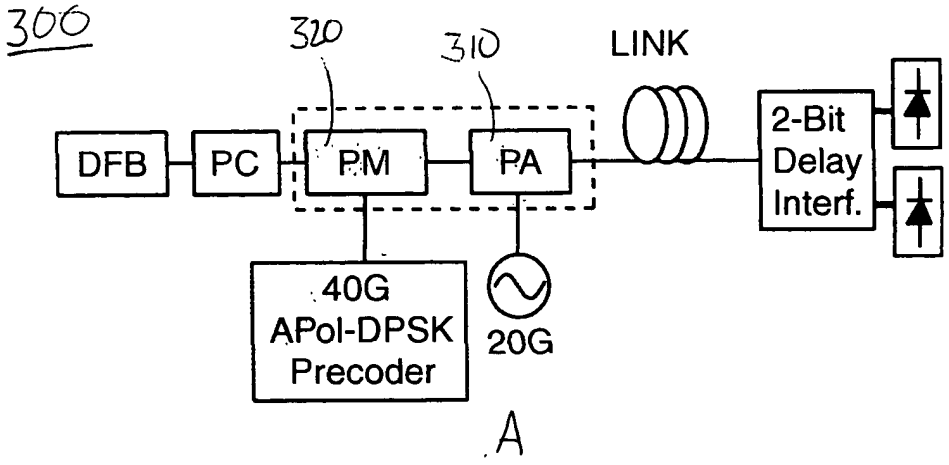
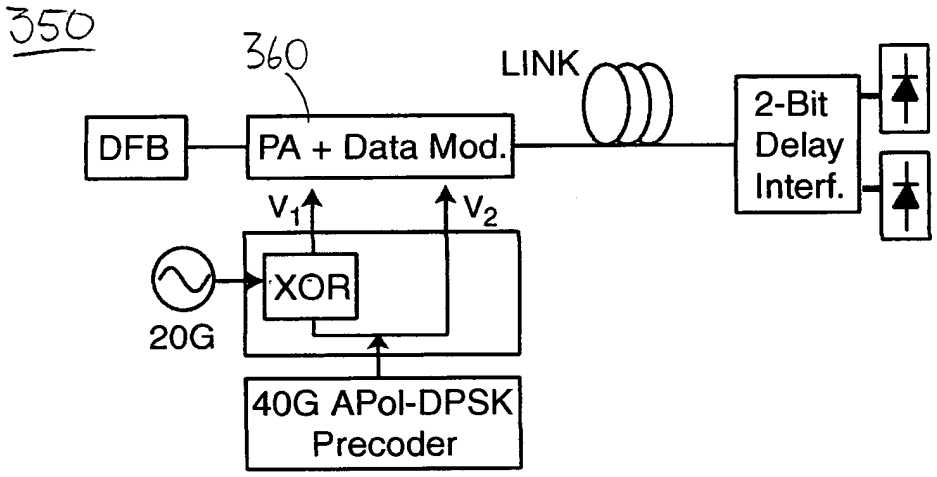

40G
Data
AND
T-FF
20G
AND
T-FF
40G
Precoded
Data
A
10G Data
10G Data
10G Data
10G Data
AND
T-FF
20G
AND
T-FF
40G
Precoded
Data
B

Figure 3


300
320
310
LINK
DFB
PC
PM
PA
2-Bit
Delay
Interf.
40G
APol-DPSK
Precoder
20G

A


350
360
LINK
DFB
PA + Data Mod.
2-Bit
Delay
Interf.
V1
V2
XOR
20G
40G APol-DPSK
Precoder

B

Figure 4

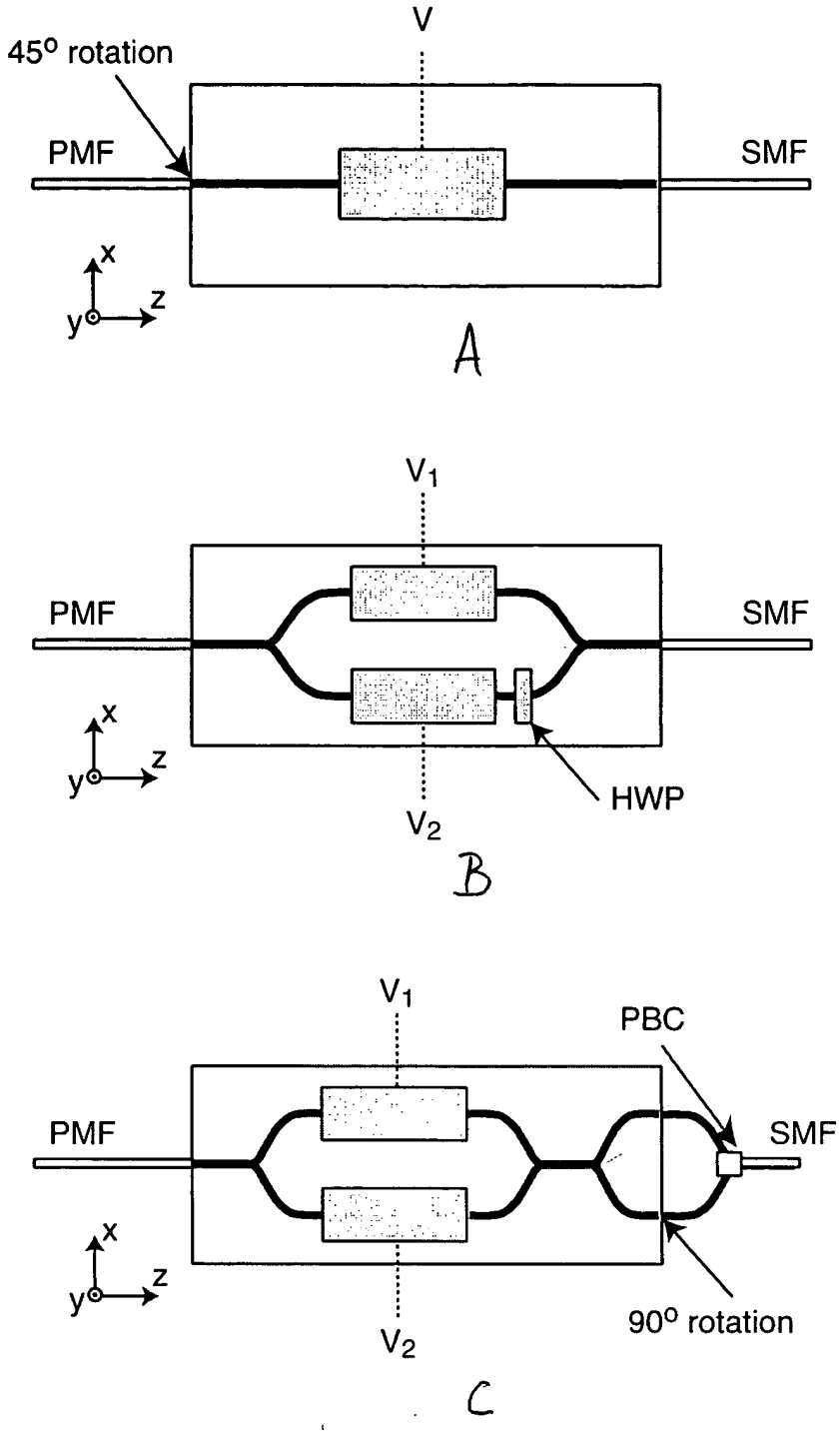

V
45° rotation
PMF
SMF
x
y
z
A
V1
PMF
SMF
x
y
z
HWP
V2
B
V1
PBC
PMF
SMF
x
y
z
90° rotation
V2
C

Figure 5

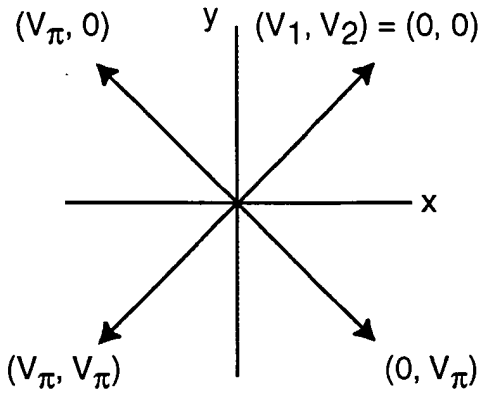


Figure 6

$D=V_2/V_\pi$	0	0	1	0	0	1	0	0
20G CLK	0	1	0	1	0	1	0	1
$D \oplus CLK=V_1/V_\pi$	0	1	1	1	0	0	0	1